

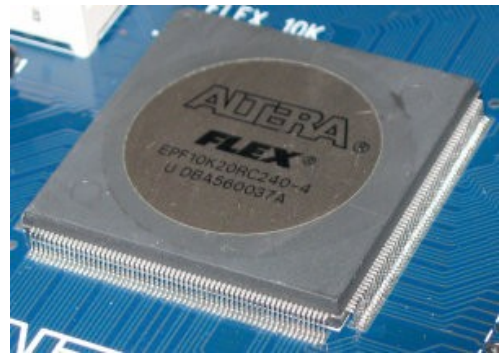


Soft CPU Cores for FPGA

In this article popular RISC CPU cores suitable for FPGA implementation are described and compared (LEON, OpenRISC, MicroBlaze, Nios II, Cortex-M1 and others).

Introduction

FPGA (Field Programmable Gate Array) devices are particularly suitable for parallel algorithms implementation. However, sequential algorithms, especially those that don't demand huge processing power, are easier to implement as a program for a microprocessor.



In many applications it would be convenient to have both a microprocessor and an FPGA array. Of course, one can have a separate RISC CPU and FPGA chips.

But they can be also combined in one chip, leading to less power consumption, simpler board layout and fewer problems with signal integrity and EMI (electromagnetic interference).

Soft CPU cores are usually used to create an FPGA-based system-on-chip (SoC). In this case a CPU core controls the work of the circuit and does some random calculations, and the other parts of the circuit are responsible for interfacing and parallel processing.

Hard vs Soft CPU Cores

There are two types of CPU cores for FPGA: *hard* and *soft*. *Hard CPU core* is a dedicated part of the integrated circuit, whereas *soft CPU core* is implemented utilizing general-purpose FPGA logic cells.

Examples of FPGA chips with embedded hard CPU cores include:

- Xilinx *Virtex-4 FX* and *Virtex-5 FXT* with PowerPC cores,
- Atmel FPSLIC with an AVR core.

Altera used to have an *Excalibur* family with embedded hard ARMv4 core, but it is now discontinued in favor of Altera's *Nios-II* soft CPU core and *Cortex-M1* ARMv6-based CPU core.

Embedded CPU soft cores suitable for FPGA

CPU core	Architecture	Bits	License	Pipeline depth	Cycles per instruction ¹	MMU ²	MUL ³	FPU ⁴	Area (LEs ⁵)	Comments
S1 Core	SPARC-v9	64	Open-source (GPL)	6	1	+	+	+	37000 - 60000	Single-core version of UltraSPARC T1
LEON3	SPARC-v8	32	Open-source (GPL)	7	1	+	+	+	3500	
LEON2	SPARC-v8	32	Open-source (LGPL)	5	1	+	+	ext	5000	Unmaintained in favor of LEON3
OpenRISC 1200	OpenRISC 1000	32	Open-source (LGPL)	5	1	+	+	-	6000	
MicroBlaze	MicroBlaze	32	Proprietary	3, 5	1	opt	opt	opt	1324	Limited to Xilinx devices
aeMB	MicroBlaze	32	Open-source (LGPL)	3	1	-	opt	-	2536	Open-source clones of MicroBlaze
OpenFire	MicroBlaze	32	Open-source (MIT)	3	1	-	opt	-	1928	
Nios II/f	Nios II	32	Proprietary	6	1	+	+	opt	1800	Limited to Altera devices
Nios II/s	Nios II	32	Proprietary	5	1	-	+	opt	1170	
Nios II/e	Nios II	32	Proprietary	no	6	-	-	opt	390	
LatticeMico32	LatticeMico32	32	Open-source	6	1	-	opt	-	1984	Not limited to Lattice devices (can be used elsewhere)
Cortex-M1	ARMv6	32	Proprietary	3	1	-	+	-	2600	
DSPuva16	DSPuva16	16	Open-source	no	4	-	+	-	510	
PicoBlaze	PicoBlaze	8	Proprietary, free	no	2	-	-	-	192	Limited to Xilinx devices
PacoBlaze	PicoBlaze	8	Open-source (BSD)	no	2	-	-	-	204	An open-source clone of PicoBlaze
LatticeMico8	LatticeMico8	8	Open-source	no	2	-	-	-	200	Not limited to Lattice devices (can be used elsewhere)

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- 1 The specified value can be valid for most of the instructions, but not for all. For example, multiplication often takes more cycles than an ordinary ALU instruction.
 - 2 Memory Management Unit.
 - 3 Hardware multiplier.
 - 4 Floating-point unit.
 - 5 Area is measured in Logic Elements (LEs) which consist from a 4-input LUT and a flip-flop. The provided area estimates are for reference purposes only.

S1 Core

S1 Core is an open-source implementation of the SPARCv9 architecture.



On March 21, 2006 Sun Microsystems, the developer of the SPARC architecture, released their *UltraSPARC T1* microprocessor to public under the terms of the GNU General Public License (GPL).

UltraSPARC T1 was an 8-core implementation of the SPARCv9 64-bit architecture, designed to run in power-critical environments.

UltraSPARC T1 itself is too huge to be implemented on FPGA. *S1 Core* is a cut-down version of the UltraSPARC T1 containing just one CPU core and additional Wishbone bus controller. Even then, *S1 Core* occupies 37000-60000 Virtex-5 LUTs (depending on the number of supported threads and L1 cache blocks) and is probably too big for most SoC designs. Nevertheless, it is probably the only available 64-bit CPU core for FPGA.

The GPL license ensures that this core can be used for free, but it requires that you give away the source code of the whole design when distributing *S1 Core* based devices.

→ <http://www.srisc.com/?s1>

LEON3 and LEON2

LEON3 is an open-source implementation of the SPARCv8 32-bit architecture designed by *Aeroflex Gaisler AB*. It is a part of the GRLIB open-source IP core library available under the terms of the GPL.

LEON3 is a fully functional pipelined SPARCv8 processor containing an optional floating-point unit. The GRLIB library contains a lot of useful IP blocks such as bus and RAM controllers.

LEON3 uses about 3500 Virtex-4 LUTs and therefore can be easily employed in mid-to-high density applications.

The GPL license allows free usage of the LEON3 CPU core, but only in open-source hardware projects. In order to be able not to distribute sources for the whole design, a special commercial license is required from Aeroflex Gaisler.

There used to be an older LEON2 core (also SPARCv8-compliant) licensed under more permissive LGPL license that allowed to use the core in proprietary projects (though some conditions still have to be fulfilled). When this article was written, there was no link to download LEON2 on the Aeroflex Gaisler website. So 1-CORE Technologies has made LEON2 available from its website for the general public.

→ http://www.gaisler.com/cms/index.php?option=com_content&task=view&id=13&Itemid=53

→ <http://www.1-core.com/resources/>

OpenRISC 1200

OpenRISC 1200 is an open-source 32-bit processing core that implements the *OpenRISC 1000* RISC architecture (there is no mistake: the core is called “OpenRISC 1200” and the architecture “OpenRISC 1000”).

OpenRISC 1200 CPU has been developed by the OpenCores.org community.

The OpenRISC architecture uses a 5-stage pipeline and its own instruction set.

GNU toolchain and Linux operating system has been ported to the OpenRISC architecture.

OpenRISC 1200 is available under the terms of the LGPL license, making it possible to use it in proprietary projects.

→ http://www.opencores.org/projects.cgi/web/or1k/openrisc_1200

MicroBlaze and its clones

MicroBlaze is a proprietary 32-bit RISC architecture and soft CPU core designed by Xilinx for use in their FPGAs.

The logo for MicroBlaze, featuring the word "MicroBlaze" in a bold, sans-serif font. "Micro" is in black and "Blaze" is in red with a white outline. A horizontal gradient bar is positioned behind the text.

There are also open-source clones of MicroBlaze, namely

aeMB and *OpenFire*, which are device-independent and binary compatible with the original.

Being developed specially for FPGA, MicroBlaze designs occupy a few times less area than LEON or OpenRISC-based designs, making it particularly suitable for mid-density FPGAs.

It should be noted that the original MicroBlaze implements features unsupported by the open-source clones, such as floating-point unit or 5-stage pipeline (open-source clones implement only 3-stage pipeline).

There is a port of the *μClinux* operating system to the MicroBlaze architecture.

→ http://www.xilinx.com/products/design_resources/proc_central/microblaze.htm

→ <http://www.opencores.org/projects.cgi/web/aemb/overview>

→ <http://www.ccm.ece.vt.edu/~scraven/openfire.html>

Nios II

Nios II is a proprietary 32-bit RISC architecture and a processor core developed by Altera for use in their FPGAs. It is a successor to the older 16-bit *Nios* embedded processor.



Nios II soft core comes in three flavors:

1. *Nios II/f* – optimized for maximum performance, it employs a 6-stage pipeline, executes 1 instruction per cycle and includes separate instruction and data caches, MMU (Memory Management Unit) and MPU (Memory Protection Unit), hardware multiply, divide and shift operations.
2. *Nios II/s* – designed as a trade-off, it employs 5-stage pipeline, executes 1 instruction per cycle and includes instruction cache (no data cache) and hardware multiply, divide and shift operations (MMU and MPU are absent).
3. *Nios II/e* – designed to occupy as little area as possible, it doesn't use pipeline, executes one instruction in 6 cycles and no supplementary arithmetic blocks.

Number of logic elements occupied by Nios II core is comparable to that of MicroBlaze, except Nios II/e edition which uses significantly less logic elements.

Nios II can only be used on Altera FPGAs (or Altera *HardCopy* structured ASICs).

GNU toolchain and Linux operating system has been ported to Nios II.

→ <http://www.altera.com/products/ip/processors/nios2/ni2-index.html>

LatticeMico32

LatticeMico32 is an open-source 32-bit RISC architecture and a CPU core developed by Lattice



Semiconductor. It should be noted that unlike Xilinx and Altera, Lattice created a portable design that can be used on other manufacturers' FPGAs or even on an ASIC.

Otherwise it is comparable to MicroBlaze and Nios II/s, being designed with the FPGA architecture in mind.

LatticeMico32 doesn't include a floating-point unit.

GNU toolchain and Linux operating system has been ported to LatticeMico32 architecture.

→ <http://www.latticesemi.com/products/intellectualproperty/ipcores/mico32/index.cfm>

Cortex-M1

Cortex-M1 is an implementation of the proprietary 32-bit ARMv6 architecture designed for FPGA. Using Cortex-M1 requires license from *ARM Limited*. There are Actel flash-based FPGA chips which are shipped with Cortex-M1 license included (no additional license is required). Cortex-M1 can be used with Xilinx and Altera FPGAs as well.



ARM (Advanced RISC Machine) is a popular RISC architecture particularly suitable for applications that demands low power consumption.

Many operating systems has been ported to ARM, including Linux and Windows CE.

→ http://www.arm.com/products/CPUs/ARM_Cortex-M1.html

→ <http://www.actel.com/products/mpu/CortexM1/>

→ http://www.altera.com/products/ip/processors/32_16bit/m-arm-cortex-m1.html

DSPuva16

DSPuva16 is an open-source 16-bit RISC core designed by Santiago de Pablo, University of Valladolid. It has an interesting feature of having a dedicated hardware multiplier-accumulator (MAC) and still occupying small area, making it possible to use it even in low-density FPGAs.

The downside is that the CPU supports quite a small program memory and no data memory (except internal registers). This processor therefore can be utilized to implement simple algorithms that nevertheless include many multiplication operations. One possible application is automatic control.

By the moment when this article was written, the original project homepage has been unavailable for a long time. 1-CORE Technologies has made DSPuva16 available from its website for the general public.

→ <http://www.dte.eis.uva.es/OpenProjects/OpenDSP/index.htm> – seems to be unavailable for a long time

→ <http://www.1-core.com/resources/>

PicoBlaze

PicoBlaze is a proprietary (but zero-cost) 8-bit RISC architecture and a CPU core developed by Xilinx.



Although available free of charge, the core is tied to a Xilinx architecture. There is also an open-source clone named *PacoBlaze*, which is a device-independent CPU core binary-compatible with the original PicoBlaze.

PicoBlaze was designed to operate in low-density FPGAs and occupy about 100 Spartan/Virtex slices.

→ <http://www.xilinx.com/products/ipcenter/picoblaze-S3-V2-Pro.htm>

→ <http://bleyer.org/pacoblaze/>

LatticeMico8



LatticeMico8 is an open-source 8-bit RISC architecture and a CPU core developed by Lattice Semiconductor and written in device-independent HDL (i.e., not tied to Lattice FPGAs).

It is quite comparable with PicoBlaze.

→ <http://www.latticesemi.com/products/intellectualproperty/referencedesigns/8bitmicrocontrollermico8.cfm>

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